Advanced Analog Integrated Circuits

Precision Techniques

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Topics

- Offset
- Drift
- 1/f Noise
- Mismatch

Motivation

1) CMOS diff pair
1 … 10 mV offset

BJT / JFET 10x better 100 μV

2) ADC 1 V full scale, 16 Bits

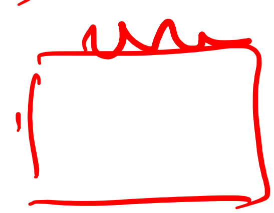
$\Rightarrow$ LSB $= \frac{1V}{2^{16}} = 15\mu V$

3) E.g. Thermometer $V_t = \frac{kT}{q}$

$\frac{\Delta V}{\Delta T} = 86 \mu V/°C$

Sources of Inaccuracies in ICs

- Systematic
  - Circuit topology (D/SE)
  - Layout (dir of current flow, proximity)
  - Stress (package, metal)
  - Volt drop (mirror)
- Random
  - Comp edge



  - Drift (T, humidity, aging, CMRR, PSRR)
  - 1/f (flicker) noise

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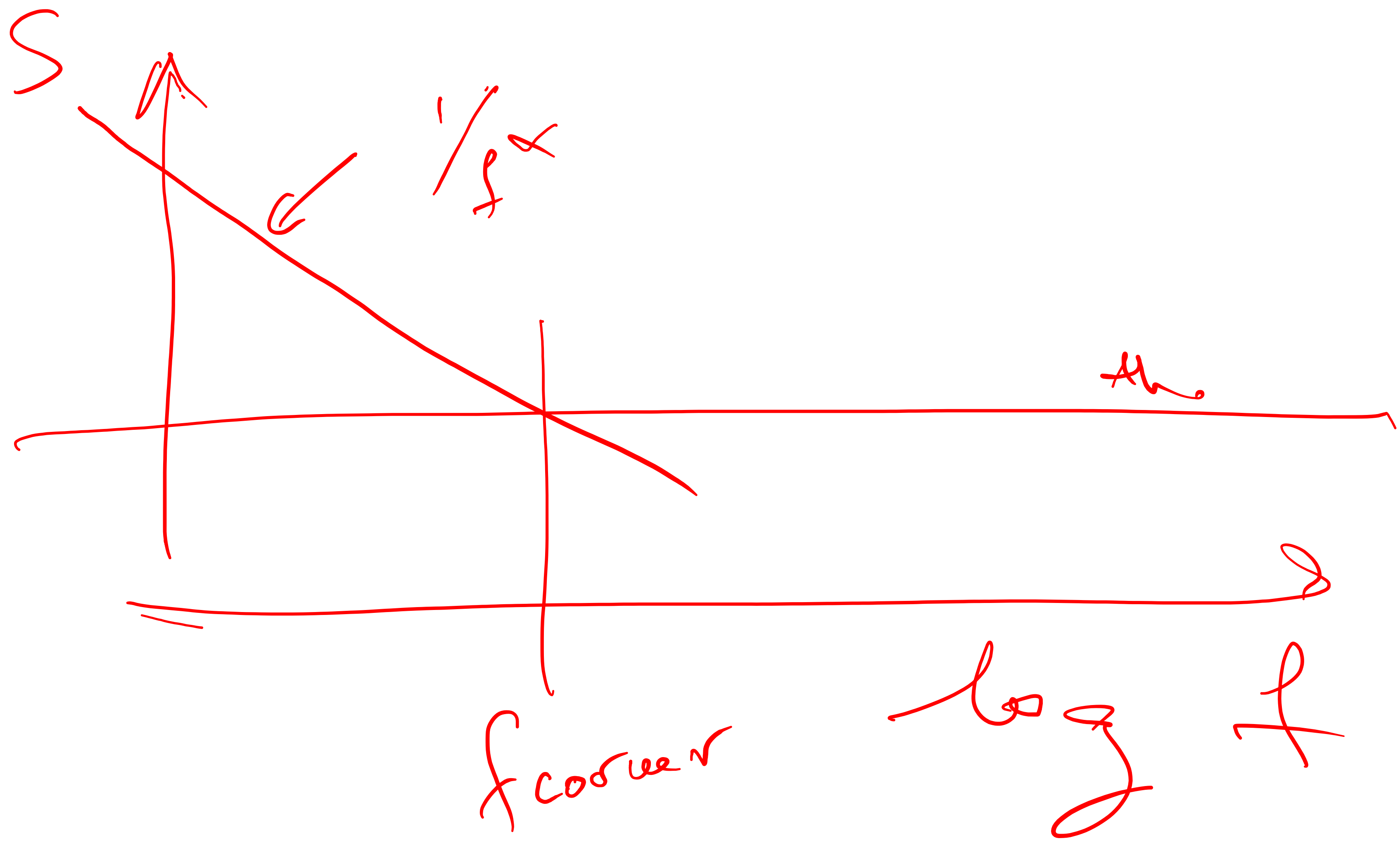
1/f Noise

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

1/f Noise Spectrum



1/f Noise

- Other names: flicker noise, pink noise
- Caused by traps near Si/SiO2 interface
  - Randomly capture and release carriers
  - Less significant in BJT, JFET, bulk current flow (PMOS)
- Empirical models:
  - D. Xie et al., "SPICE Models for Flicker Noise in n-MOSFETs from Subthreshold to Strong Inversion," IEEE Trans. CAD, Nov 200, pp. 1293-1303.
  - $\overline{i_{1/f}^2} = \frac{K_f I_d}{C_{ox} L^2} \frac{\Delta f}{f}$
- K_f is technology dependent, numbers for EE 240B:

	180nm Process	65nm Process
NMOS	$4 \cdot 10^{-29} \mathrm{A} \cdot \mathrm{F}$	$6 \cdot 10^{-29} \mathrm{A} \cdot \mathrm{F}$
PMOS	$2 \cdot 10^{-29} \mathrm{A} \cdot \mathrm{F}$	$3 \cdot 10^{-29} \mathrm{A} \cdot \mathrm{F}$

1/f Noise Corner Frequency

1/f Noise Corner Frequency

$$\underbrace{\frac{K_f \, I_d}{C_{ox} L^2} \cdot \frac{\Delta f}{f_{co}}}_{1/f} = \underbrace{4kT\gamma \, g_m \cdot \Delta f}_{th}$$

$$\therefore f_{co} = \frac{K_f}{8kT\gamma \cdot C_{ox}} \cdot \frac{V^*}{L^2}$$

L_{min}, $V^* \sim 150\,mV$

180nm → 0.7 MHz   65nm = 5.5 MHz

“Total” 1/f Noise

$$\overline{i_{1/f}^2} = \int_{f_1}^{f_2} \frac{K_f I_d}{C_{ox} L^2} \cdot \frac{df}{f} = \frac{K_f \cdot I_d}{C_{ox} L^2} \cdot 2.3 \log \frac{f_2}{f_1}$$

* 1 ... 10 Hz vs 1 GHz ... 10 GHz
* $f_1 = \emptyset$

$$\sqrt{\frac{f_1 = 1/\text{year}}{f_1 = 1\,\text{Hz}}} = 1.34 \rightarrow 34\%\ \text{incr.}$$

1/age of universe + 64%

Total 1/f versus Thermal Noise

$$\overline{i_{nT}^2} = 4kT\gamma \cdot g_m \left(f_2 + 2.3 \cdot f_{co} \cdot \log \frac{f_2}{f_1} \right)$$

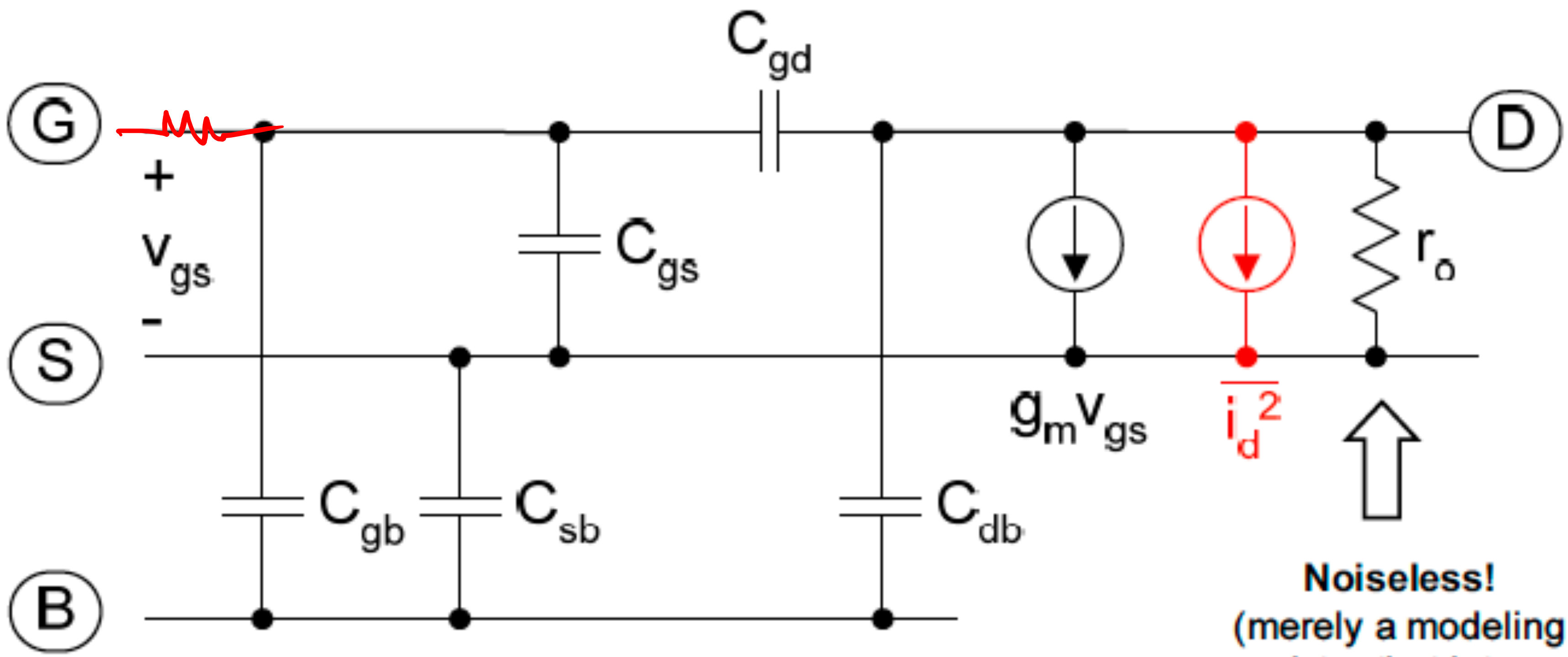
f_2: th; $2.3 \cdot f_{co} \cdot \log \frac{f_2}{f_1}$: 1/f

f_2 for which $S_{thT} = S_{1/fT}$?

$$f_2 = 2.3 \cdot f_{co} \cdot \log \frac{f_2}{f_1} \approx 23 f_{co}$$

$\log \frac{f_2}{f_1} \approx 10$

MOS Model with Channel Noise Generator



Noiseless!
(merely a modeling resistor that lets us account for finite dI_D/dV_{DS})

Other MOSFET Noise Sources

- Gate Noise
  - gate leakage
  - gate resistance
  -
- Bulk noise
- Source barrier noise
- J. Jeon et al, VLSI Symp. 2009, pp. 48-49

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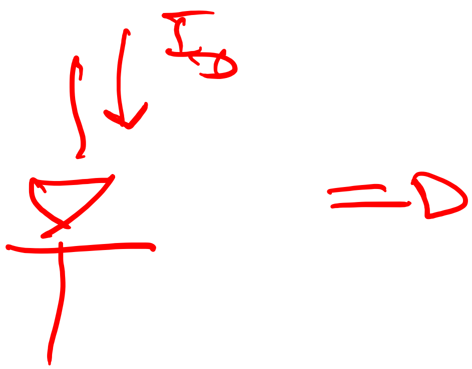
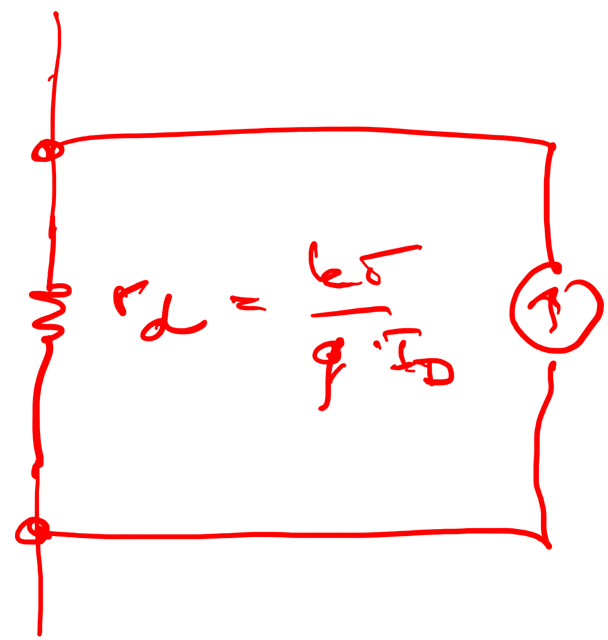
Shot Noise
(Aside …)

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Shot Noise in PN Junction

- DC current flow
- Diode
- PSD → white
- Model

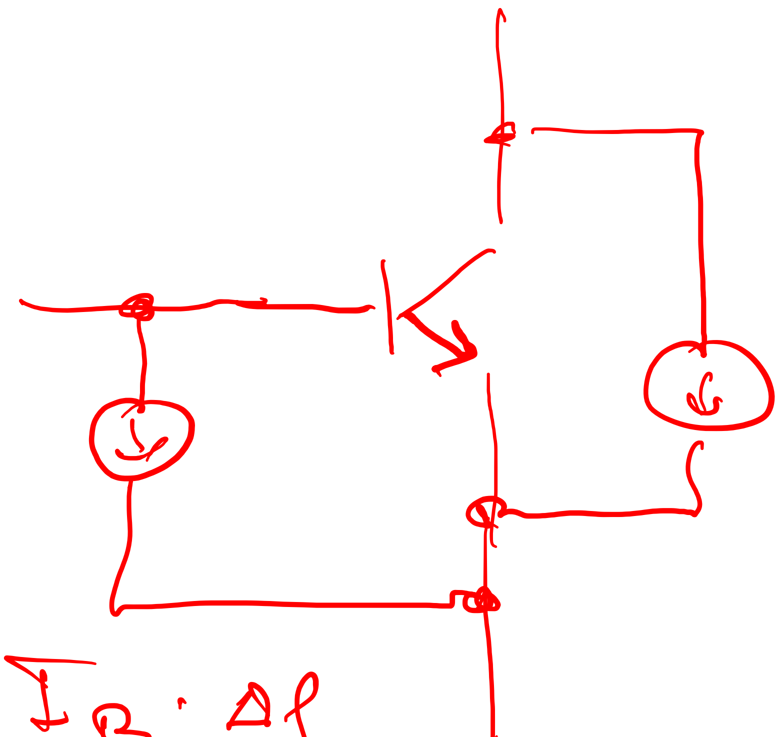




$r_d = \frac{kT}{q \cdot I_D}$

$\overline{i_{nD}^2} = 2q I_D \cdot \Delta f = 2kT \frac{1}{r_d} \cdot \Delta f$

Shot Noise in BJTs

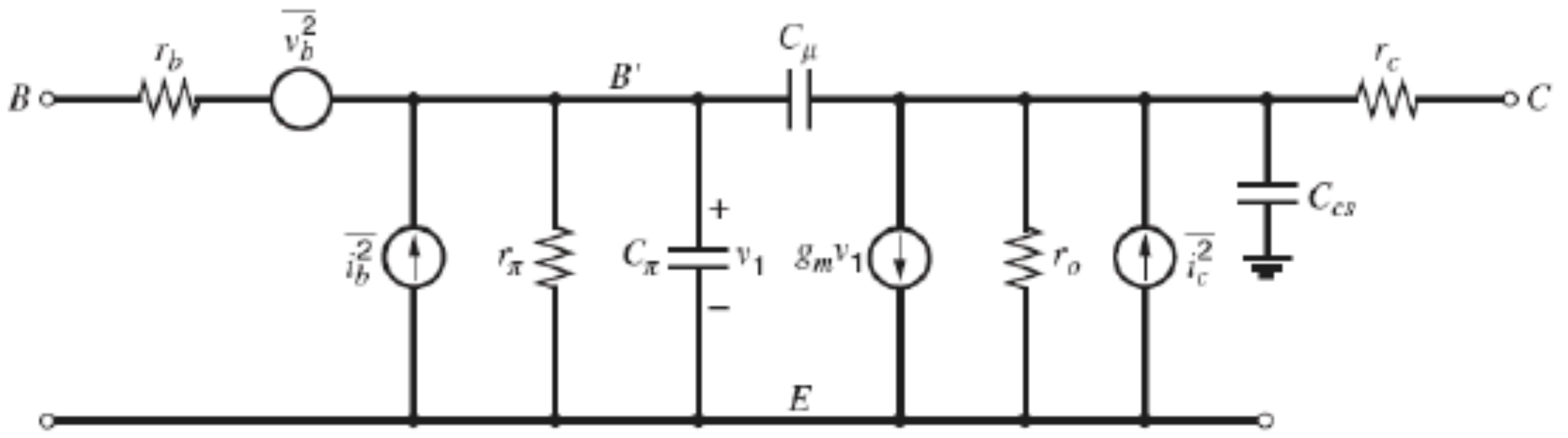


$$\overline{i_b^2} = 2q I_B \cdot \Delta f$$

$$\overline{i_c^2} = 2q I_C \cdot \Delta f = 2kT g_m \cdot \Delta f$$

uncorrelated

BJT Small Signal Noise Model



$$\overline{v_b^2} = 4kT\, r_b\, \Delta f$$

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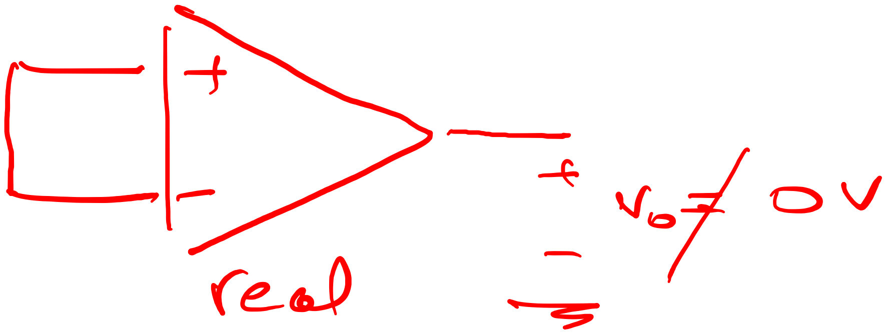
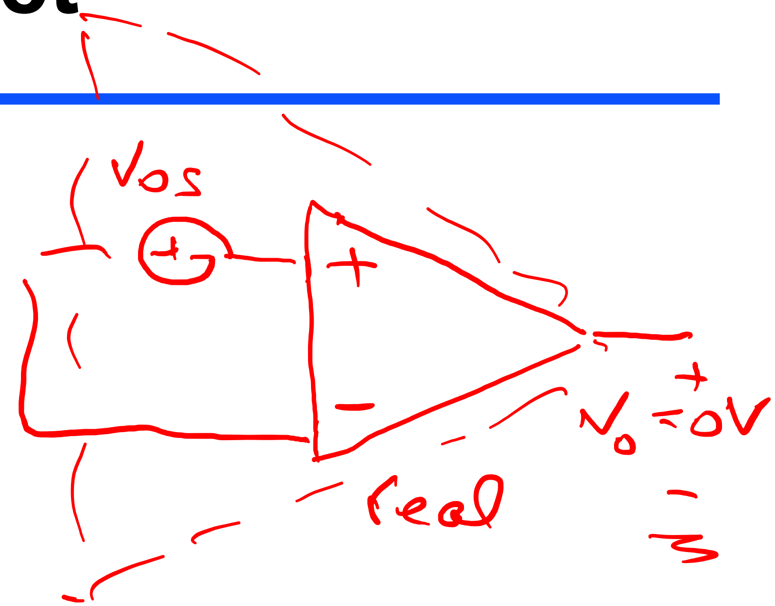
Offset

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Modeling Offset





Typical $V_{os} \approx 100\mu V$ ... $10mV$

BJT: better

ΔI_{os} ?

Sources of Error and Mitigation

- Constant
  - trim:
    - Laser trimming
    - DAC + memory
      - ↑ Flash
      - ↑ OTP
- Variable
  - 1/f – noise
  - Drift (env., stress)
  - ⇒ DOC → < 1µV
  - CMRR, PSRR

Dynamic Offset Cancellation (DOC)

2 Ideas

a) Measure & subtract

→ Auto-zeroing

→ CDS correlated double sampling

b) modulate signal out of band

→ Choppers

Refs: [1] K. Makinwa, "Dynamic offset cancellation techniques in CMOS," ISSCC Tutorial, Feb. 2007 (available from SSCS website).

[2] C.C. Enz and G.C. Temes, "Circuit techniques for reducing the effects of opamp imperfections: autozeroing, correlated double sampling and chopper stabilization," Proc. IEEE, Nov. 1996, pp. 1584 -1614.

DOC Techniques Comparison

AZ, CDS

- Discrete time
- Thermal noise folding ⇒ kT/C
- sample, subtract (2-phases)

↑ MOS

Chopping

- Cont. time
- no noise folding
- modulate offset out of band → filter

↑

DOC versus Trimming

DOC +

- Reduces const + dyn. errors (1/f)
- Good stab over temp., supply
- No added testing costs

DOC −

- Possible BW reduction (incr. power)
- Incr. complexity
- Aliasing and/or intermod.

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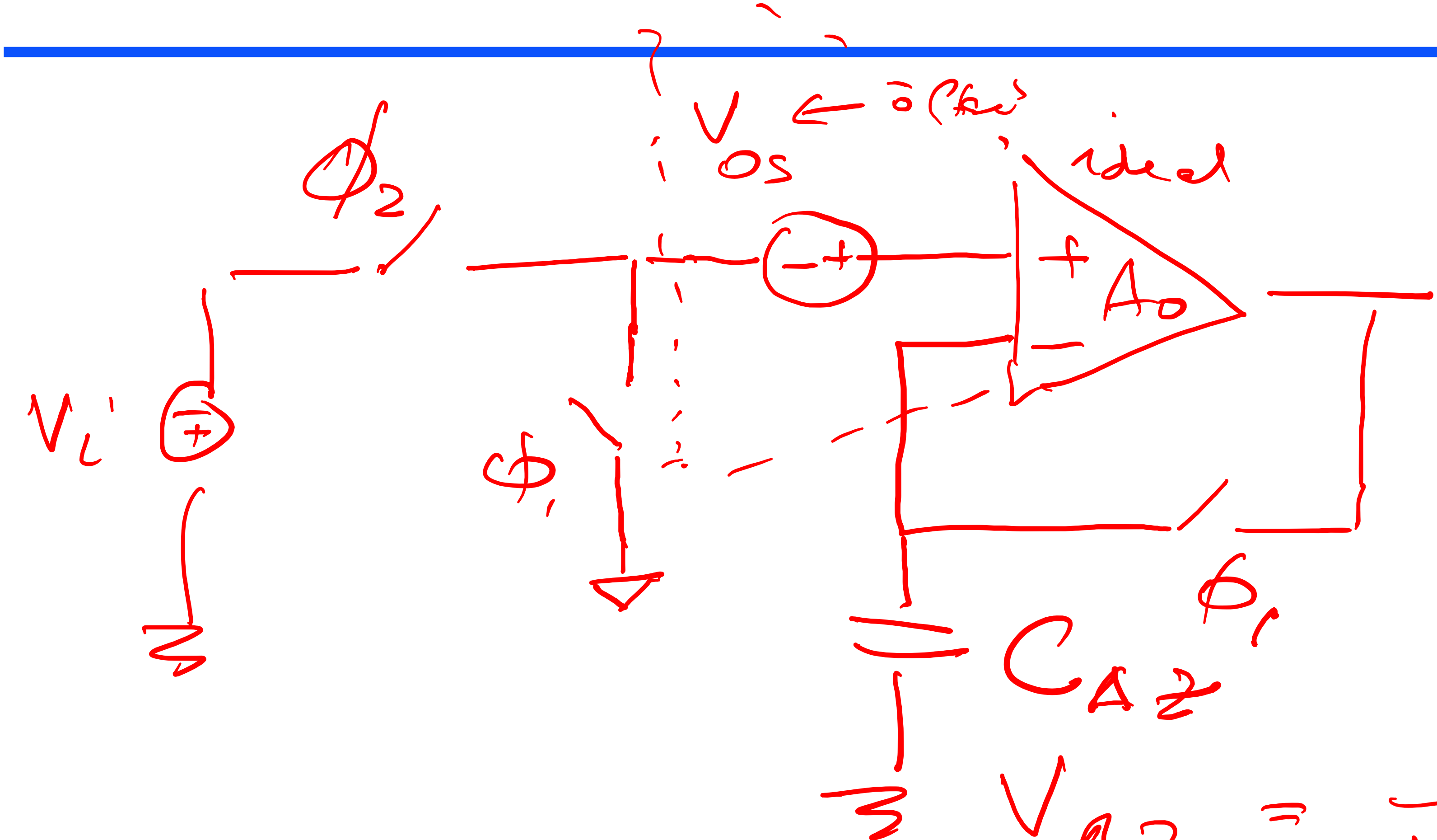
Auto Zeroing

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Auto-Zeroing Principle



$$V_{AZ} = \frac{A_o}{1 + A_o} V_{os}$$

$$V_{out} = A_o \left(V_{in} + \frac{V_{os}}{1 + A_o} \right)$$

Auto-Zero Phase Φ_1 (DC Analysis)

Amplification Phase Φ_2 (DC Analysis)

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Auto Zeroing Noise Analysis

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

What Happens to Noise?

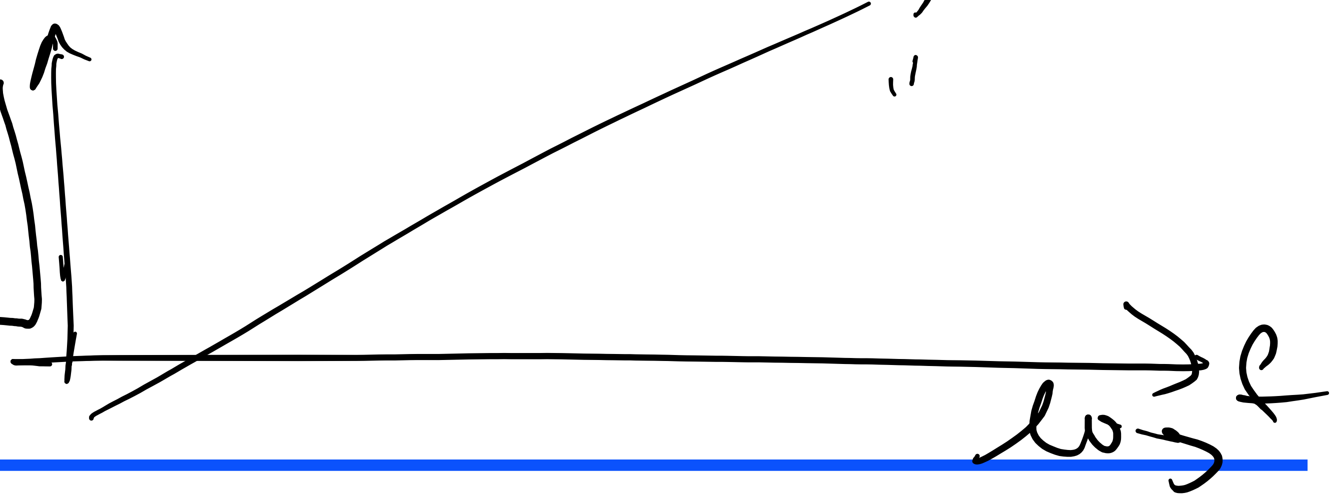
Noise Transfer Function

$$V_{o,n\,1/f}(s) = A_0 \cdot \sqrt{\overline{v_{1/f}^2}}\left(1 - e^{-sT/2}\right)$$

$$V_{o,n\,1/f}(f) = A_0\sqrt{\ } \cdot 2\sin\left(2\pi f \frac{T}{2}\right)$$

$$\cong A_0 \cdot \sqrt{\ } \cdot 2\pi f \cdot T$$

$$1/T \gg f_{co}$$



Noise Transfer Function

Noise Spectrum at Output

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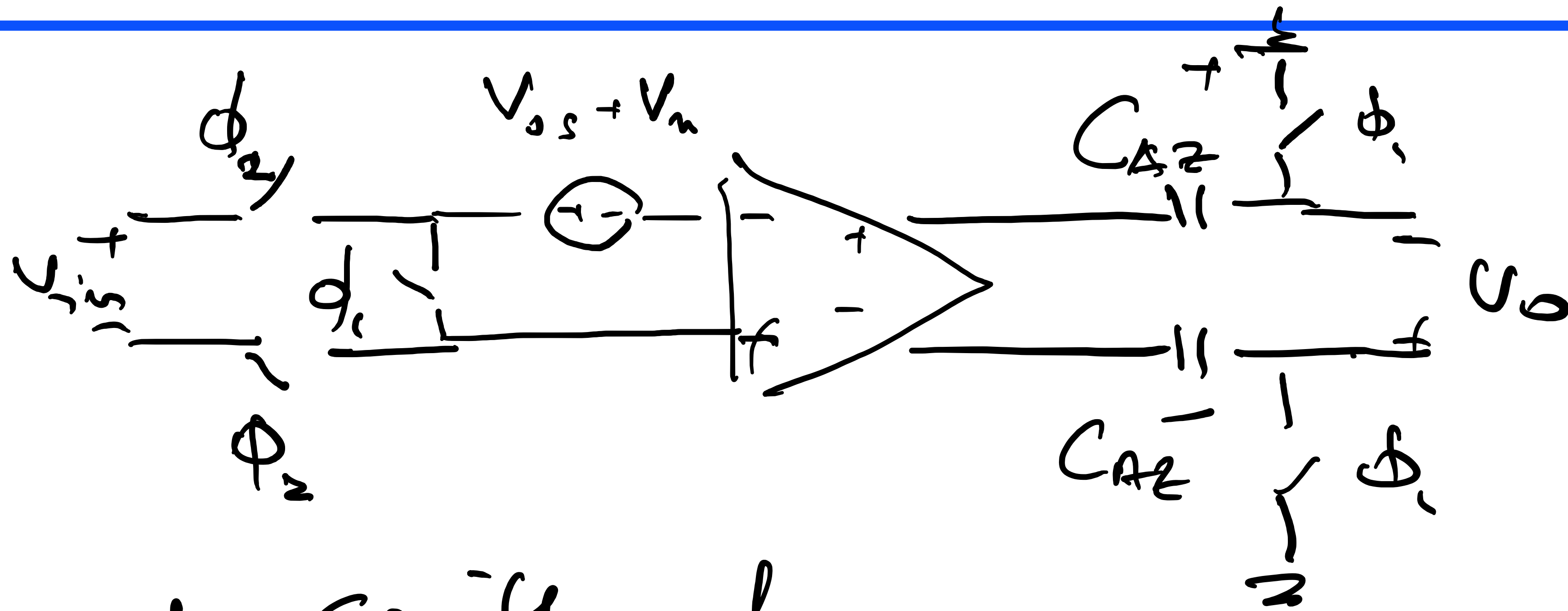
Auto Zeroing Charge Injection

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

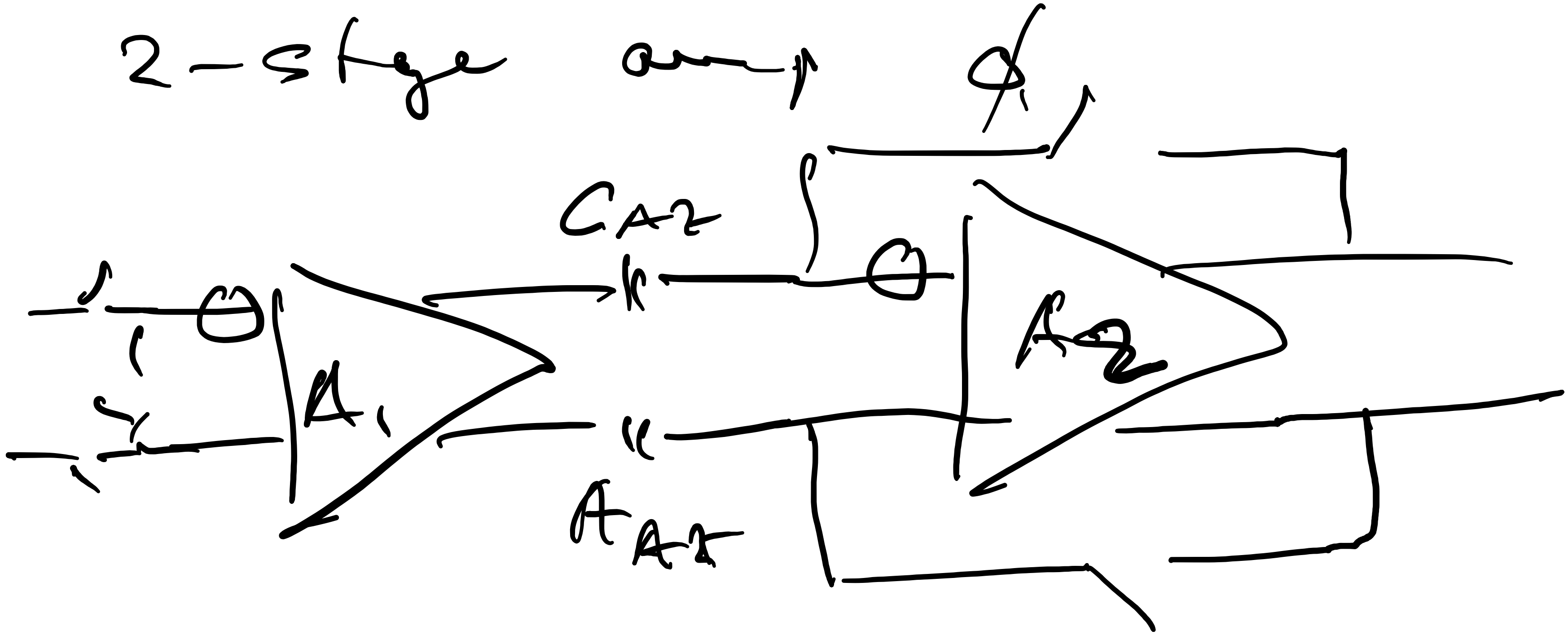
Mitigating Charge Injection Error



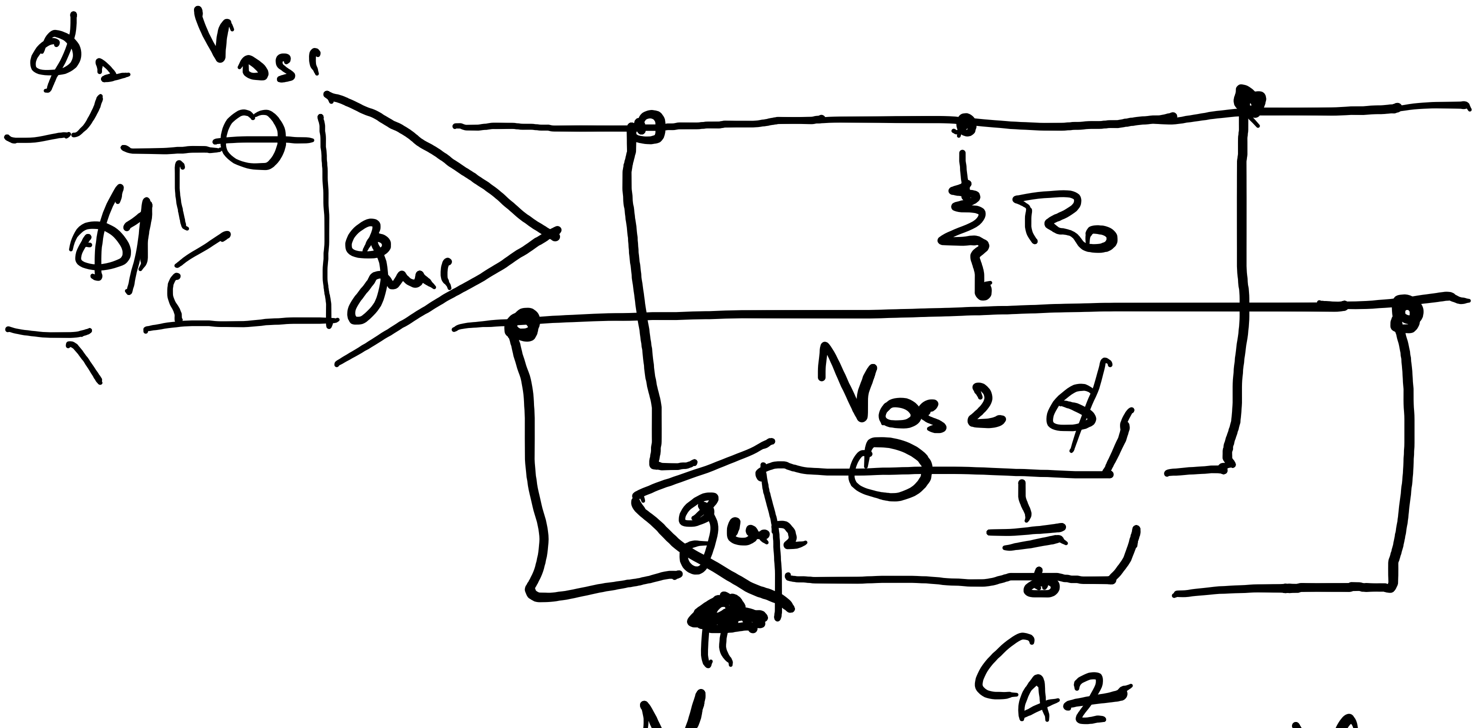
\+ switch charge injection reduced by $1/A_0$

\- railing

Reducing Charge Injection Error (1)

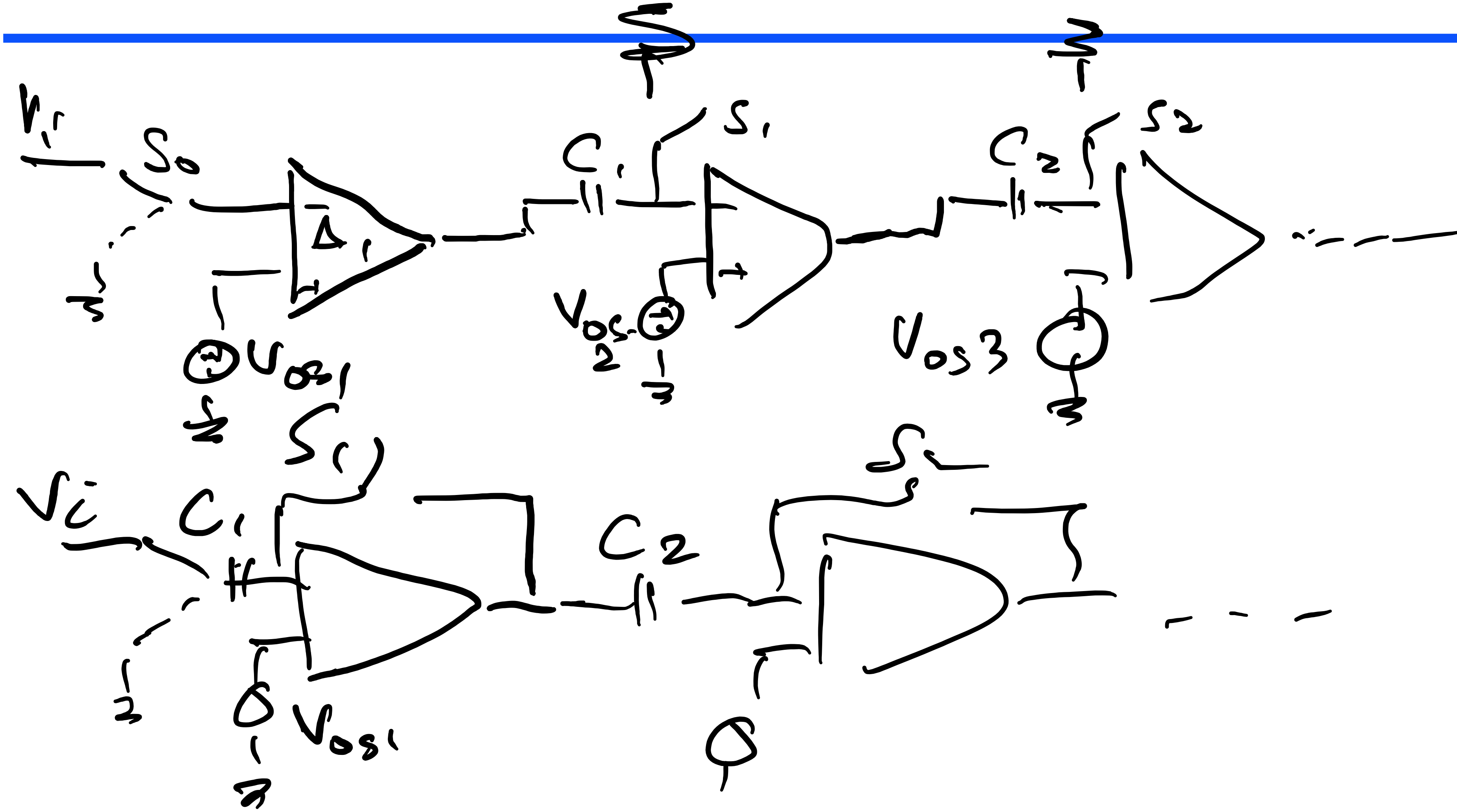


Reducing Charge Injection Error (2)



$$V_{off,res} = \frac{V_{os1}}{g_{m2} \cdot R_o} + \frac{V_{os2}}{g_{m1} \cdot R_o} + \frac{\Delta V}{g_{m1}/g_{m2}}$$

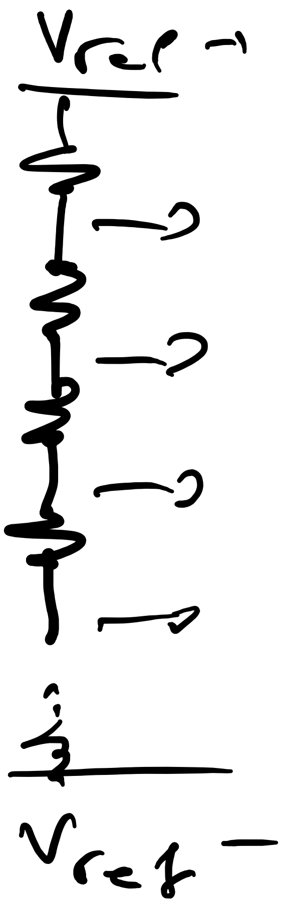
Multistage Offset Cancellation

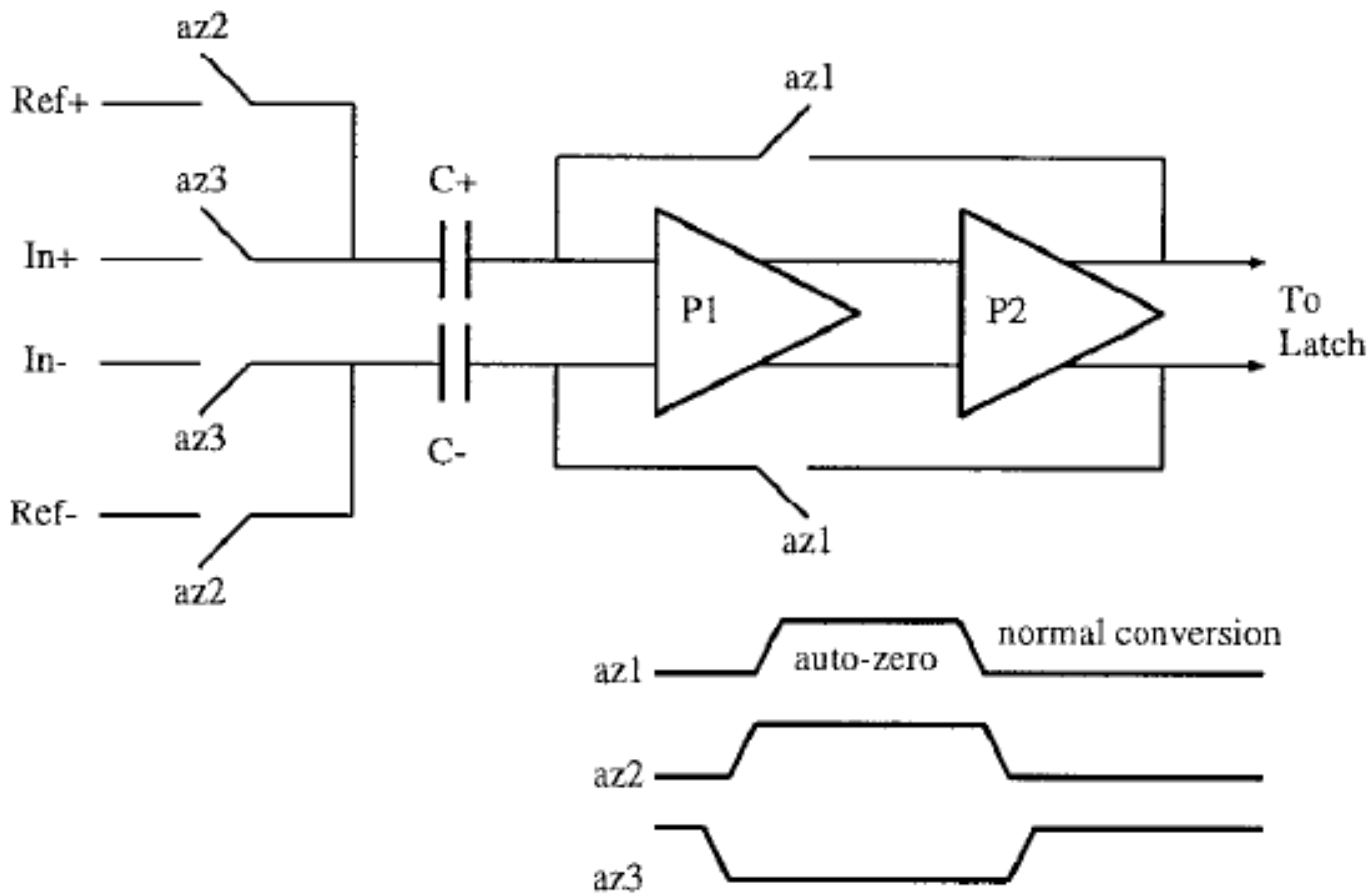


Multistage Offset Cancellation

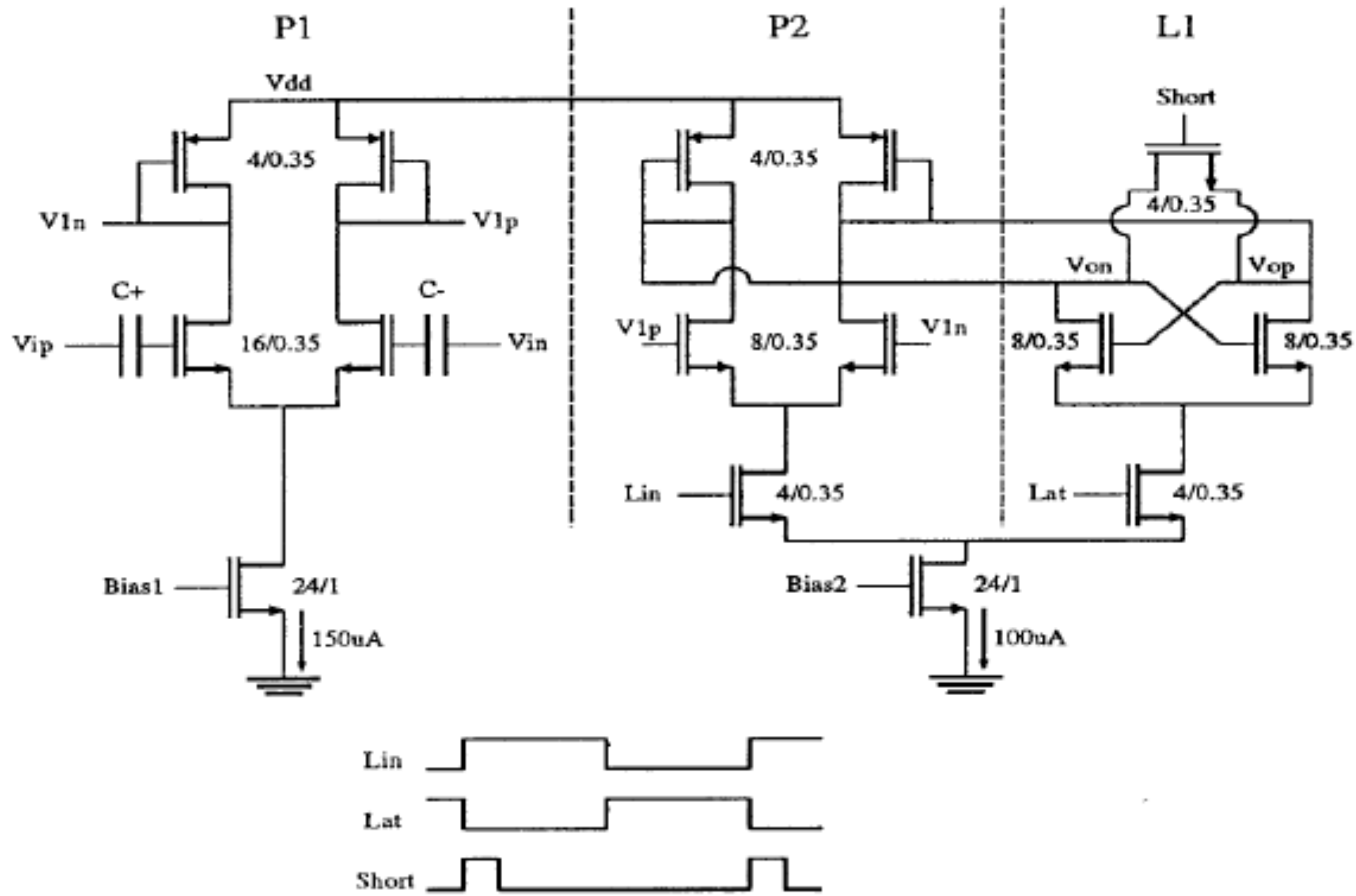
Comparator Example

- Mehr & Dalton, JSSC 7/1999





Comparator Example: Circuit Details



Auto-Zeroing Residual Offset

Residual Errors:

- switch charge injection
- leakage C_{AZ}
- Finite amp gain

residual V_{os}

1 ... 10 µV

Solutions:

- Diff ckts
- Bottom plate sampling
- small switches
- Large C_{AZ}
- High gain amps

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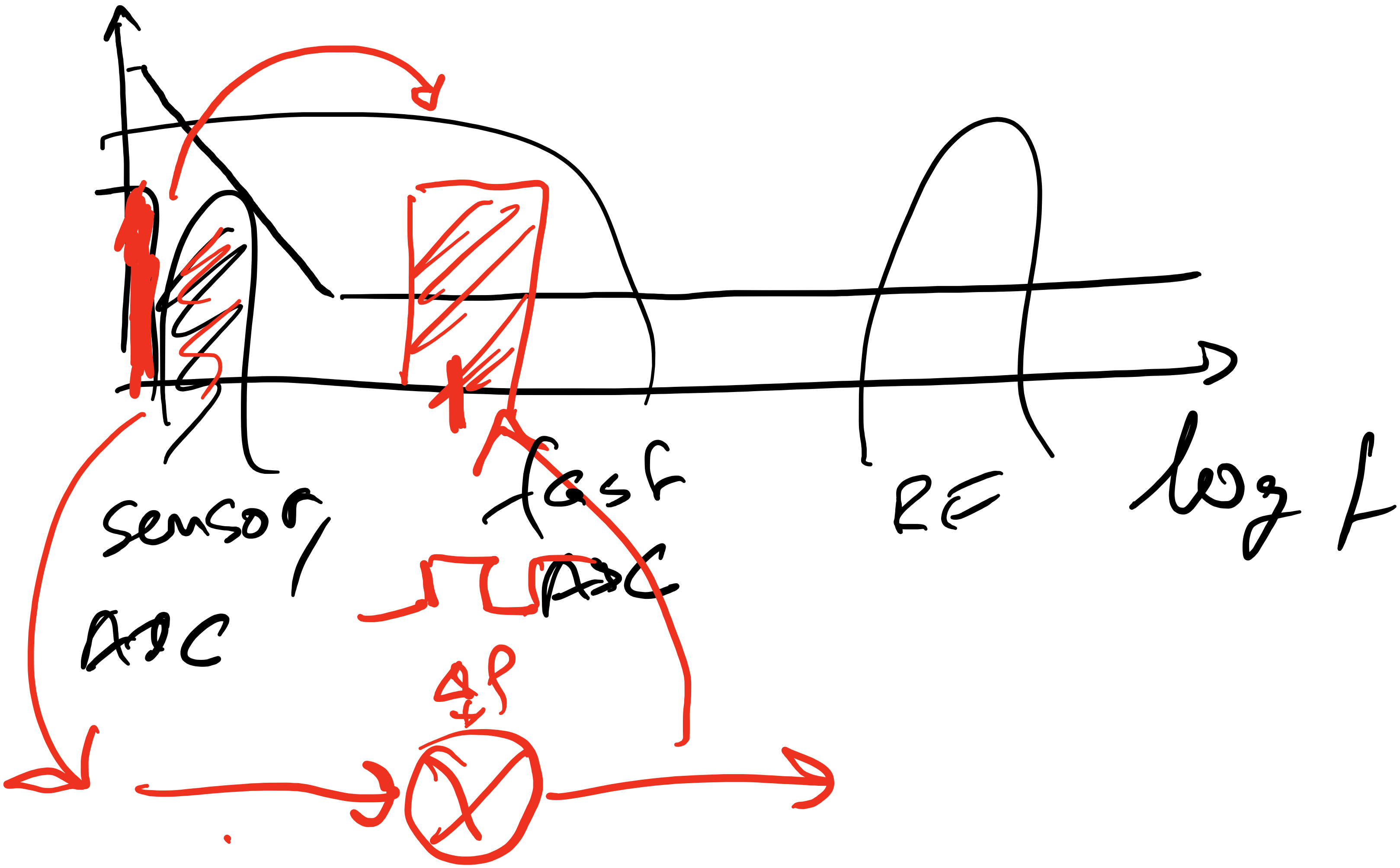
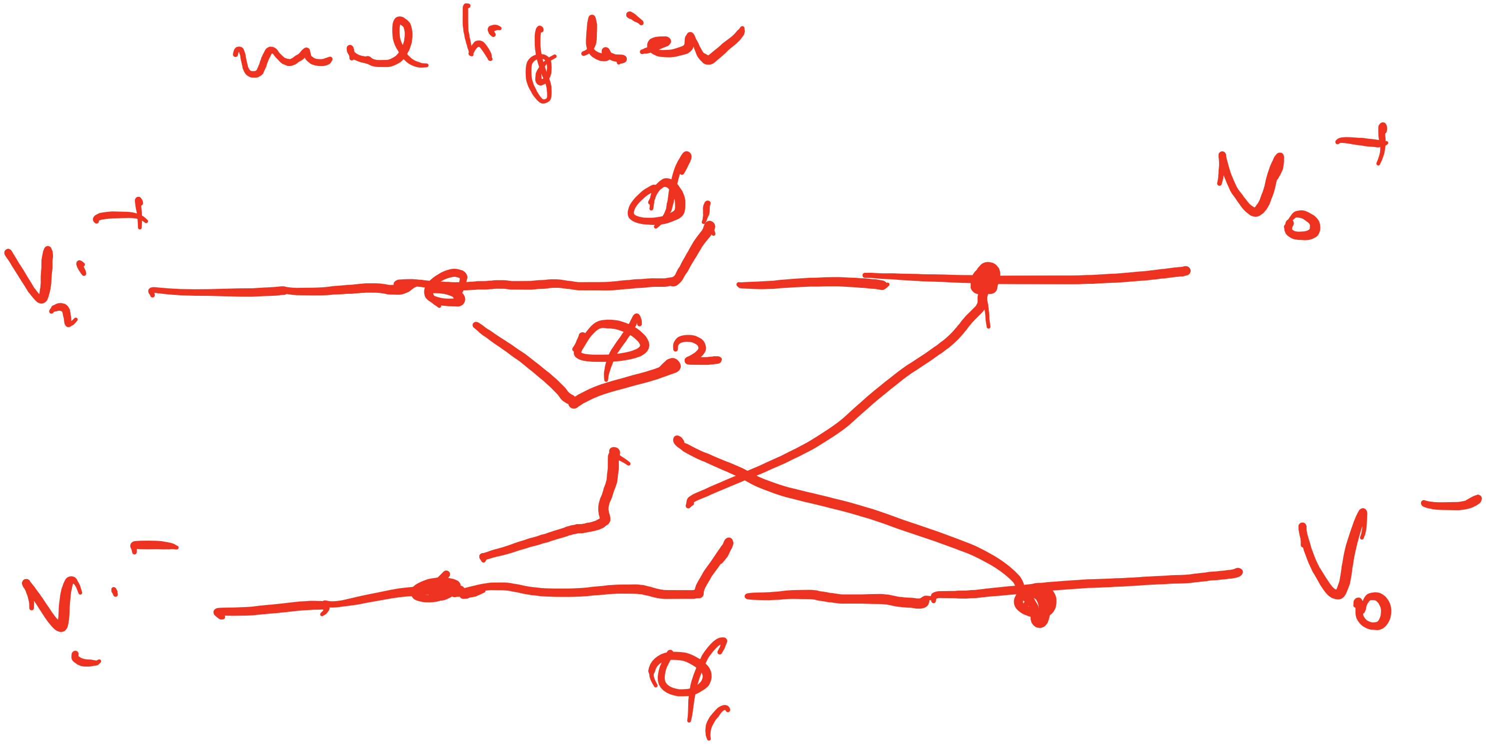
Chopper Stabilization

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Chopping Idea



Chopping Concept



Square Wave Modulator

Time Domain

Frequency Domain

Frequency Domain

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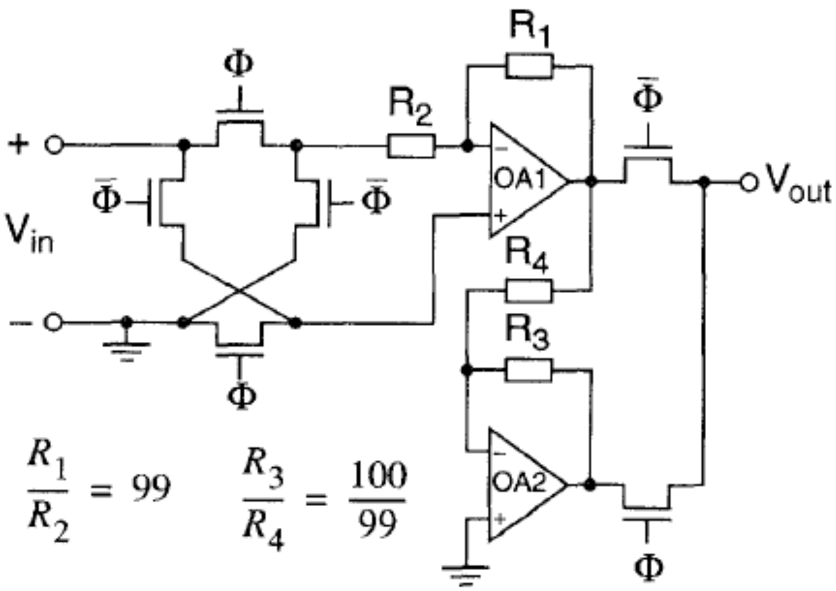
Chopper Noise

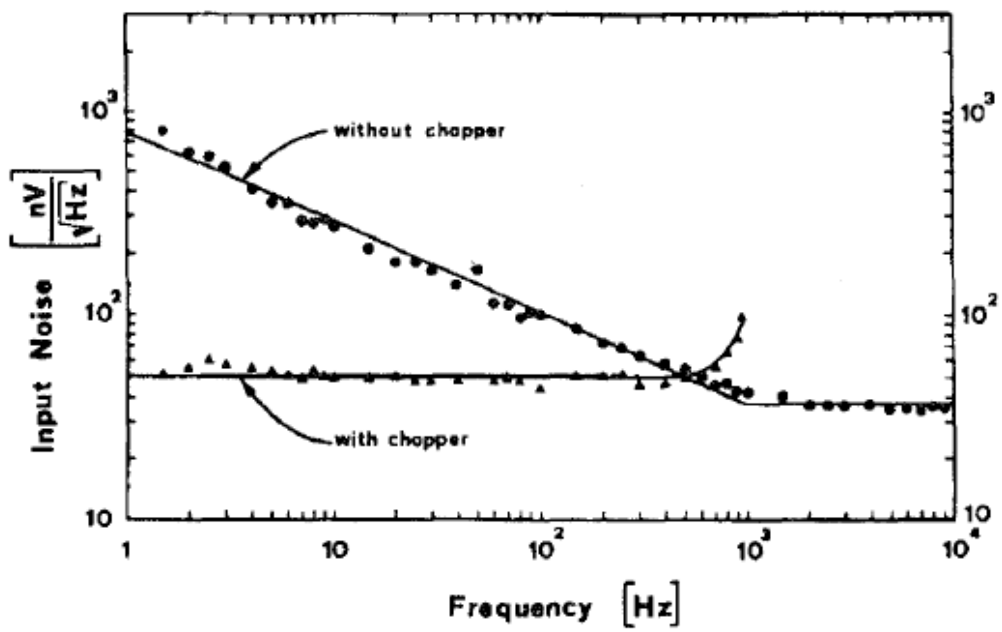
Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Residual In-Band Noise

Residual In-Band Noise

Example





[Enz 1996]

Two-Stage Chopper Amplifier

Folded Cascode with Chopper

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Chopper Nonidealities

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Finite Amplifier Bandwidth

Clock Feedthrough

Summary of Chopper Design Considerations

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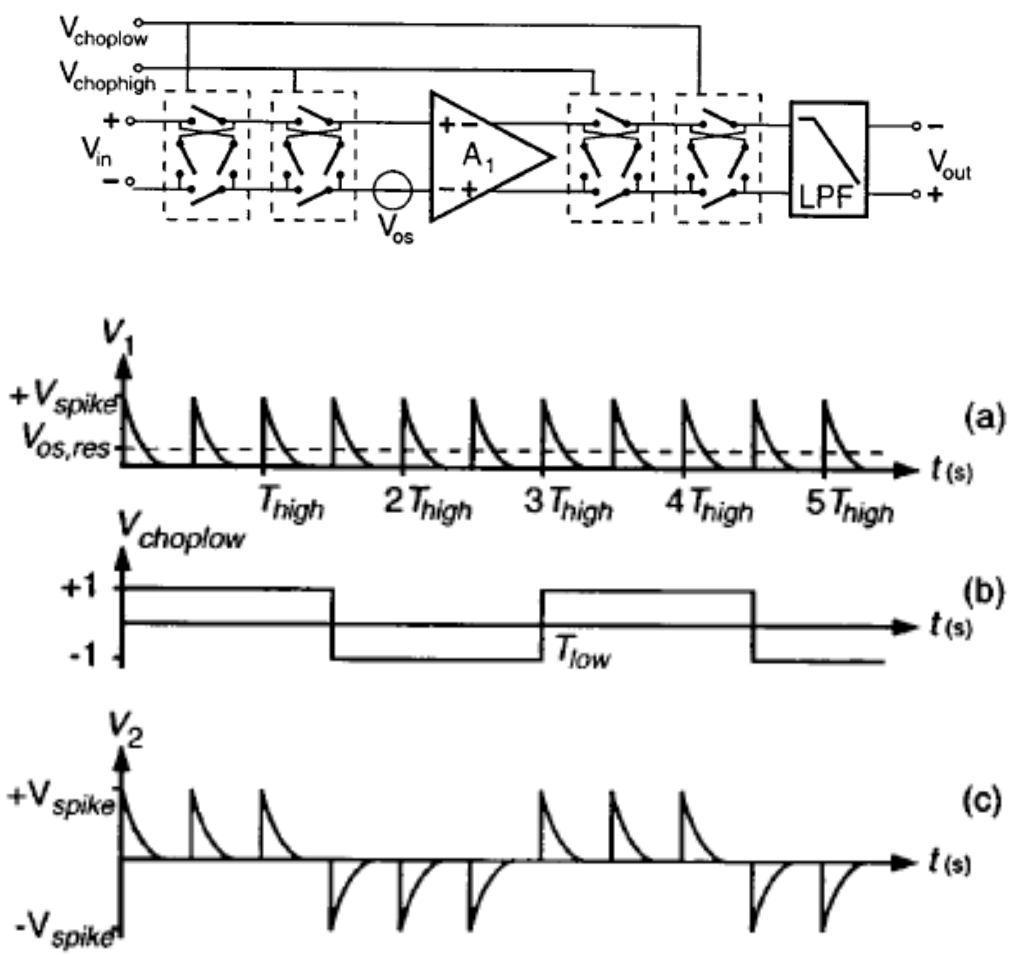
Advanced Chopping Techniques

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Objectives

Nested Chopping



[Bakker 2000]

Spike Dead-Banding

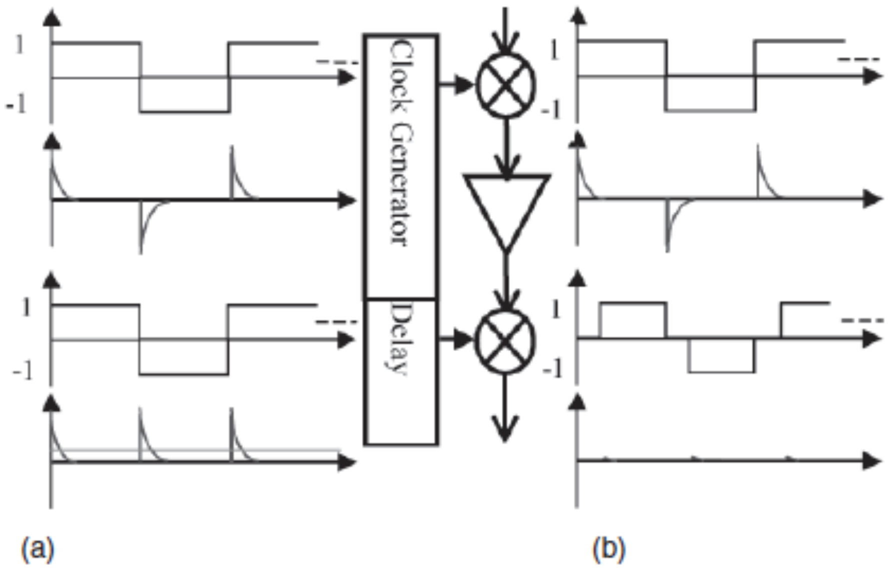
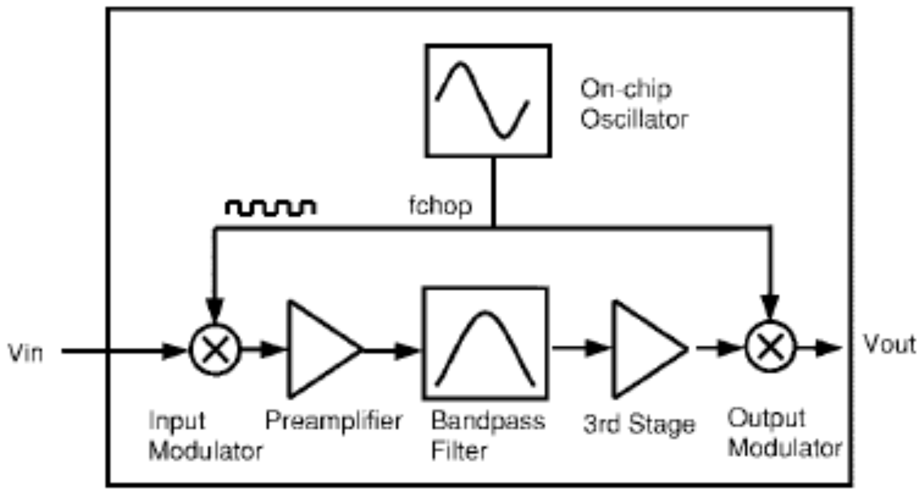


Figure 23.3.1: (a) Charge injection in conventional chopper amp. (b) Chopper amplifier with guard time.

[Menolfi 2001]

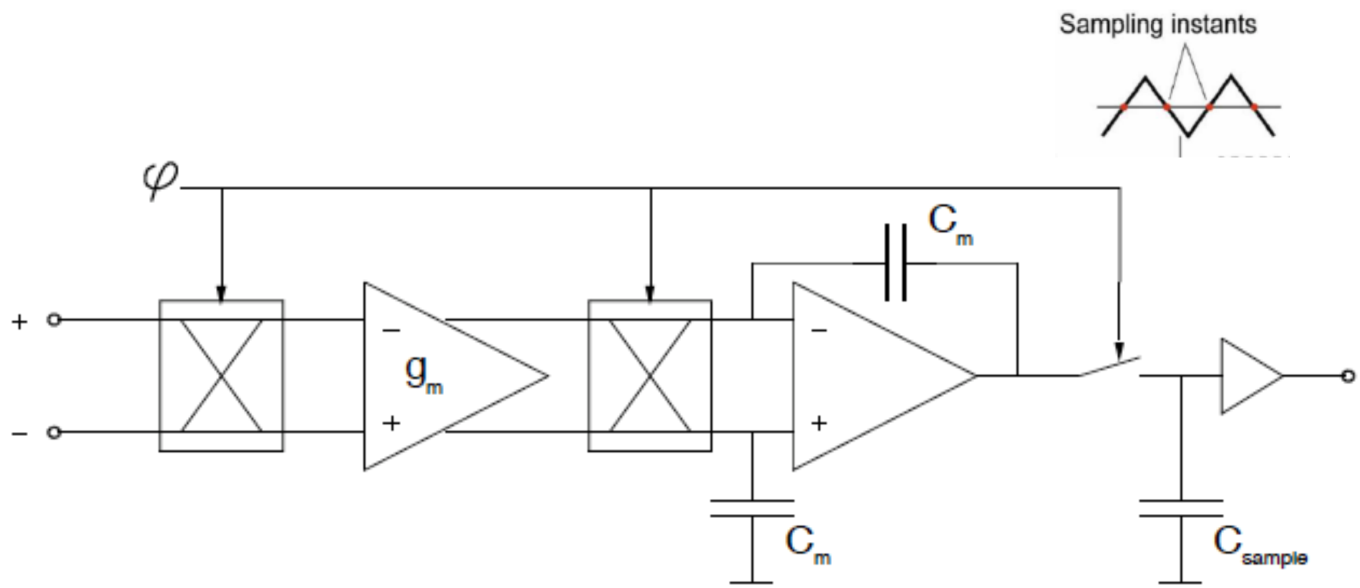
Spike Bandpass Filter



[Menolfi 1999]

Ripple Reduction with AC Coupling

Ripple Reduction with SC Filter



[Bakker 1997]

Ripple Reduction with Digital Filter

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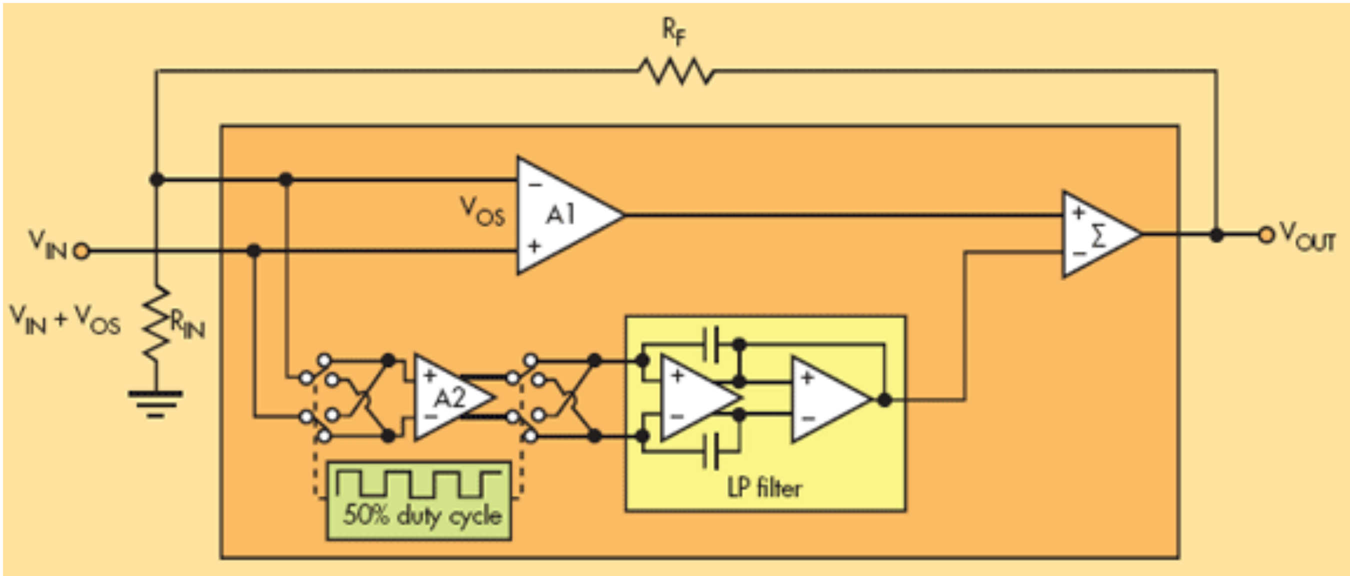
Chopper Amplifier Performance

Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

Offset Compensated OpAmps

Implementation Example



Chopper-stabilized op amps build on the classical chopper amplifier concept that was first used in vacuum tubes. Those basic choppers modulated the input signal with a square wave and demodulated the output. Thus, any low-frequency errors introduced by the amplifier were shifted outside the band of interest and filtered out by subsequent stages. In a chopper-stabilized amplifier, there is a wideband path (A1), paralleled by a high-accuracy low-frequency path (A2) that provides high gain and classic chopping. The outputs of A1 and A2 are subtracted, with the output fed back to the inverting input of A2 and to a switch on the non-inverting input of A1 that alternates at the chopping frequency between the feedback signal and the input signal. A low-pass filter between the output of A2 and the summing node circuit removes the high-frequency chopping noise. The clever bit is that connecting the inputs together allows the chopping to remove the low-frequency errors from both paths.

http://electronicdesign.com/analog/chopper-stabilized-op-amps

Chopping Summary

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Dynamic Element Matching

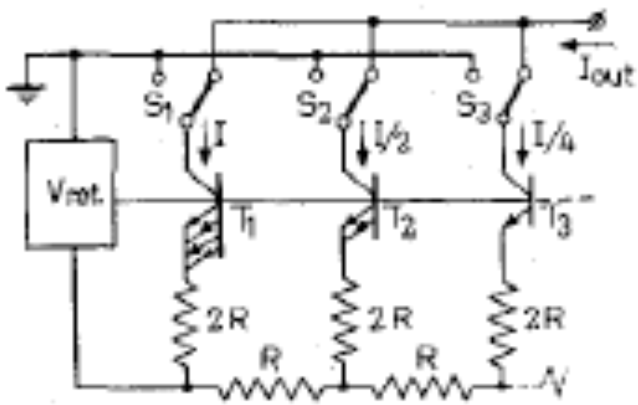
Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

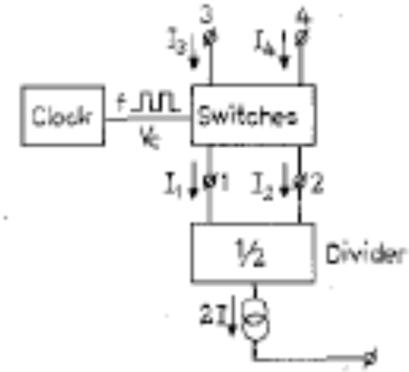
Application: Precision DAC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

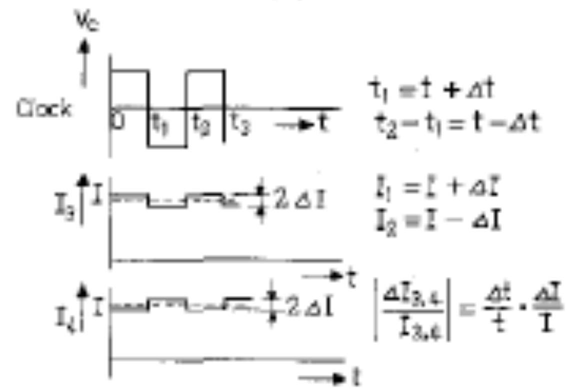
Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE





(a)



DEM Concept

DAC Application Example

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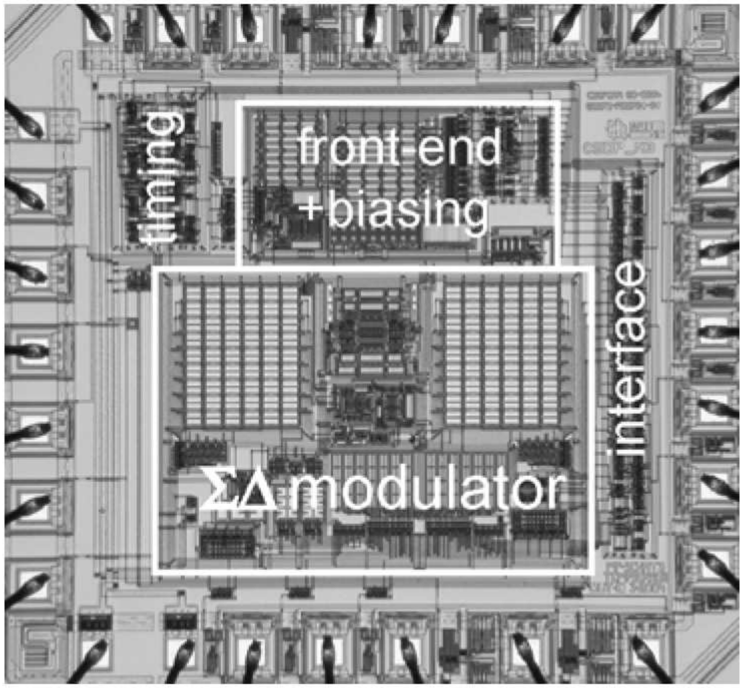
Temperature Sensor Example

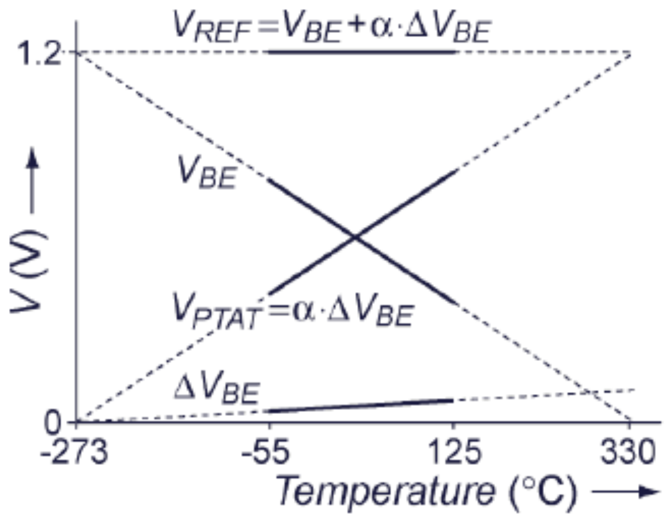
Bernhard E. Boser
University of California, Berkeley
boser@eecs.berkeley.edu

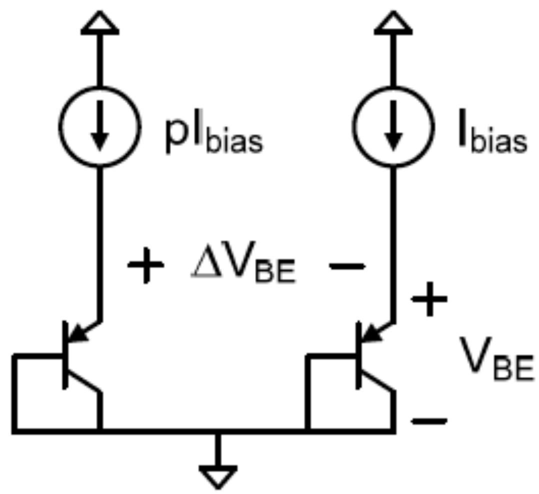
CMOS Temperature Sensor



[Pertijs 2005]

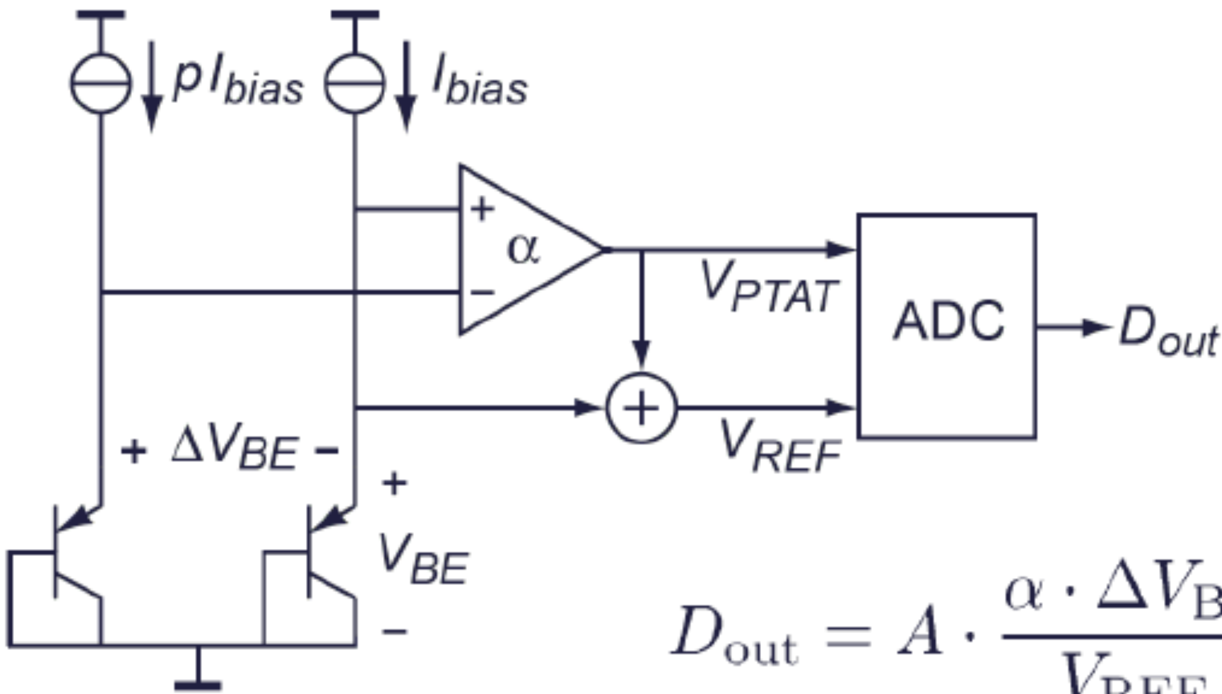
Bandgap Temperature Sensing





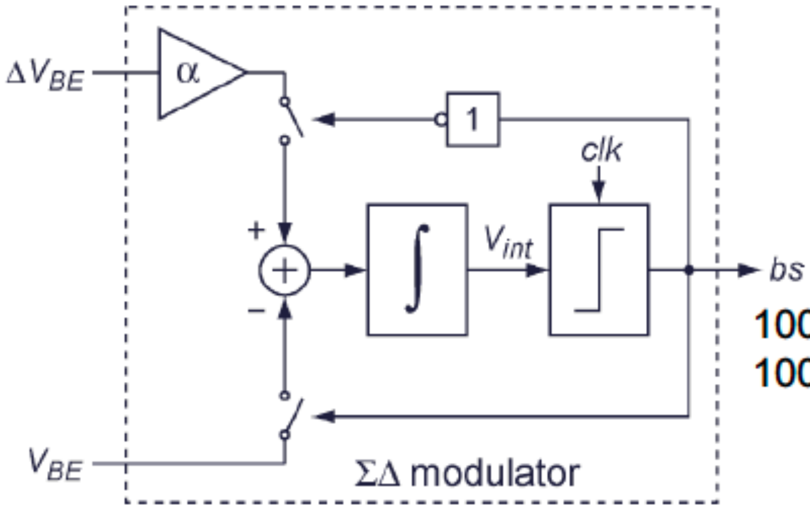
$$V_{\mathrm{BE}}(T) = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{bias}}(T)}{I_S(T)}\right) \qquad \Delta V_{\mathrm{BE}}(T) = \frac{kT}{q} \ln(p)$$

Sensor Principle



$$D_{\mathrm{out}} = A \cdot \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} - B$$

A/D Conversion: ΣΔ Modulator

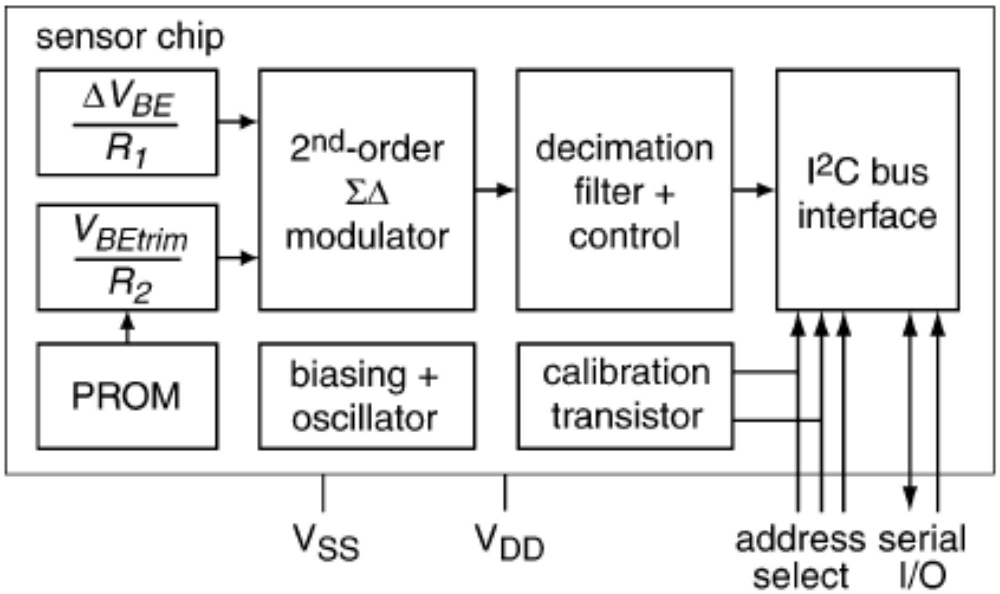


10001000
1000....

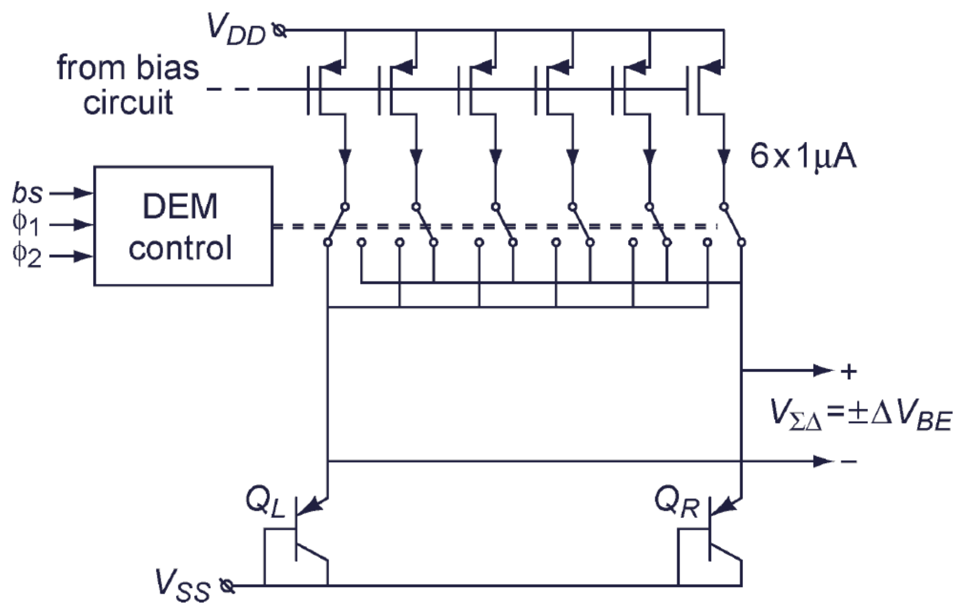
$$(1-\mu)\cdot\alpha\cdot\Delta V_{\mathrm{BE}}=\mu\cdot V_{\mathrm{BE}}$$

$$\mu=\frac{\alpha\cdot\Delta V_{\mathrm{BE}}}{V_{\mathrm{BE}}+\alpha\cdot\Delta V_{\mathrm{BE}}}=\frac{\alpha\cdot\Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}}$$

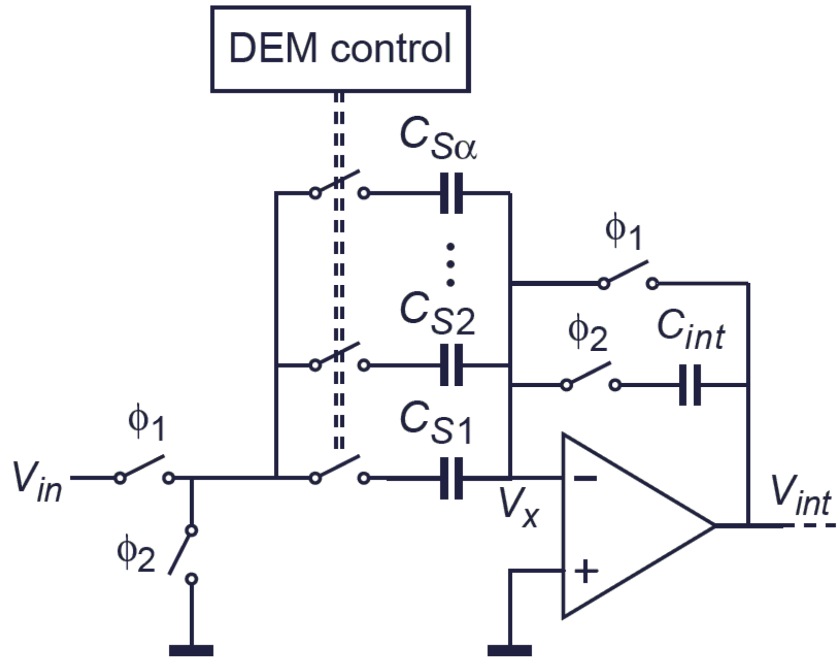
Temperature Sensor Block Diagram



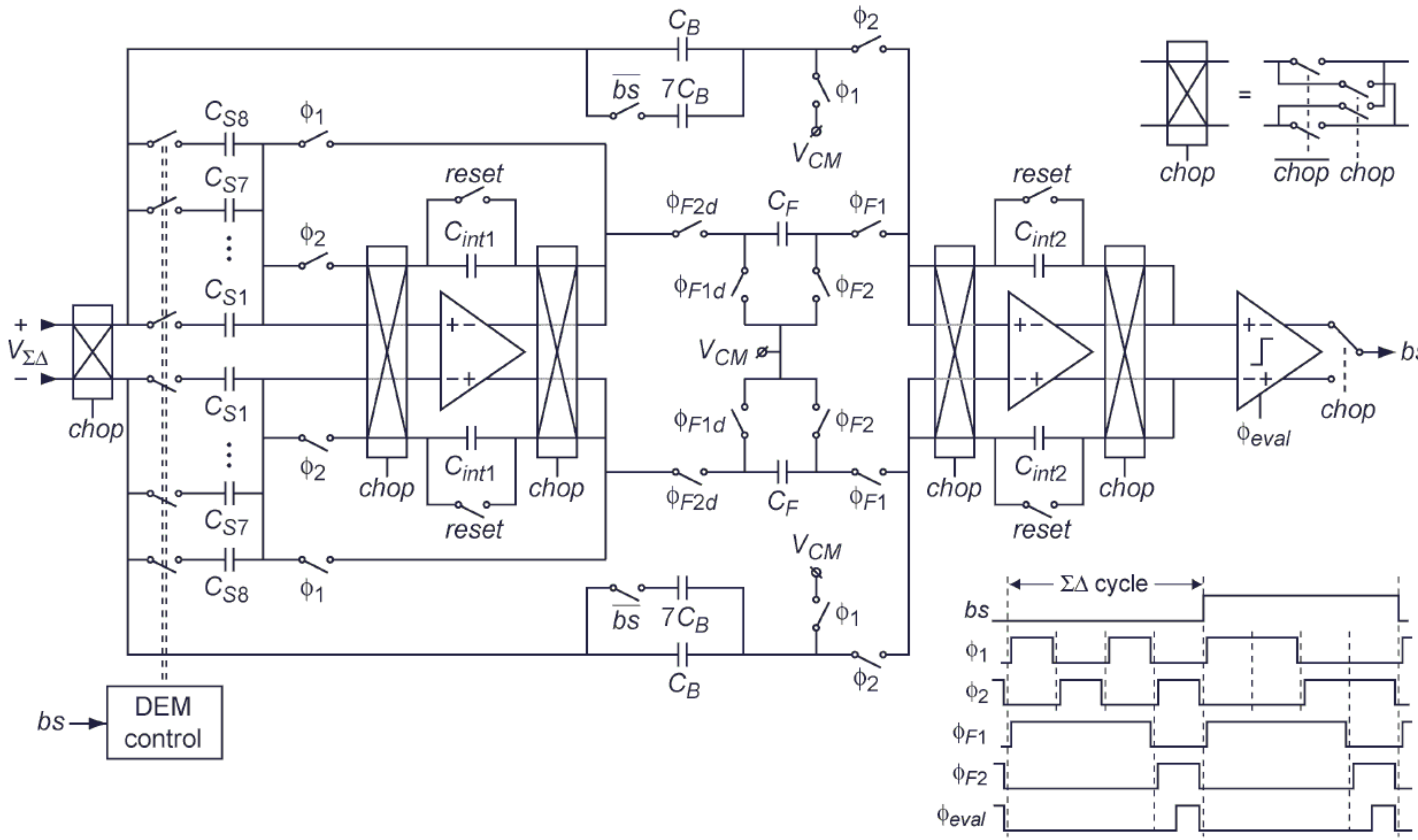
(1) Accurate 1:p Ratio with DEM



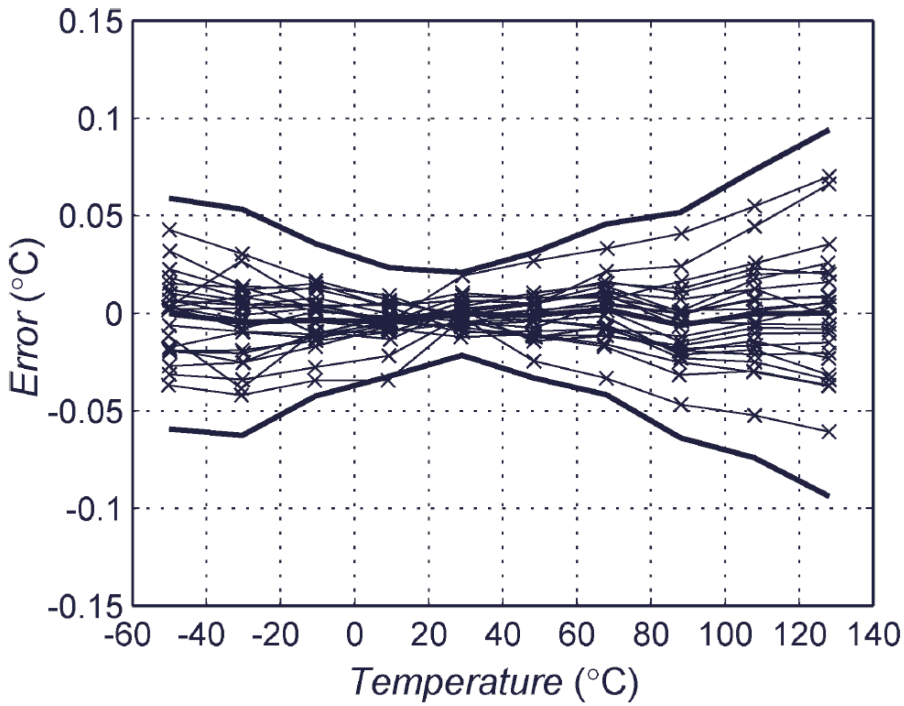
Sigma-Delta Modulator



Sigma-Delta Circuit Implementation



Evaluation



Technology	0.7μm 2M-1P analog CMOS
Chip size	4.5mm^2
Supply voltage	2.5V – 5.5V
Temperature range	$-55°$C – 125°C
Resolution	0.01°C at 10 conversions/s 0.002°C at 1 conversion/s
Supply current	75μA when operated continuously
Power-supply sensitivity	0.03°C/V from 2.5V to 5.5V
Inaccuracy (3σ)	$\pm$0.03°C at 30°C $\pm$0.1°C from -55°C to 125°C

- Other techniques used to get target performance:
  - β insensitive I_{Bias} generation
  - V_{BE} curvature correction
    - Nonlinear decimation filter
  - V_{BE} averaging between Q_L and Q_R